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10/733,693	12/11/2003	Wayne A. Britson	ROC920030248US1	8659

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IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2112	

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12/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,693	BRITSON ET AL.	
	Examiner	Art Unit	
	SAM RIZK	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 10/24/2008
- Claims 5 and 7 have been Cancelled
- Claims 1-4, 6, 8-20 have been submitted for examination
- Claims 1-4, 6 and 8-20 have been rejected

Response to Arguments

1. Applicant's arguments filed on 10/24/2008 have been fully considered but they are not persuasive.

2. In response to applicant's argument, page 10, lines (1-5), that Isom does not make any mention of a "test signal" the Examiner disagrees for two reasons:

a) Isom in column 5, lines (41-440 teaches "the redundant data path may be used to replace data path of the I/O circuit (204) which may have a fault or failure.". A person skilled in the art would recognize that in order to detect a fault or failure inherently must have some sort of test signal.

b) Even if Isom does not disclose a test signal per se, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. <u>If the prior art structure is capable of performing the intended use, and then it meets the claim.</u>

3. The Applicant in page 10, line 12 argues that Isom fails to disclose a plurality of input lines coupled to a processor. Well, Isom in Figure 3 teaches a plurality of

input lines (ref. (102) Pin (0) – Pin (N)) that is coupled to the resident IC (ref. (206) wherein Isom has defined the IC as a "processor" in col. 1, line 27.

4. The Examiner disagrees with the applicant and maintains the rejection of claims (1-4, 6 and 8-20) as in the office action mailed on 8/14/2008. All the amendments and arguments have been considered. It is the Examiner's conclusion that claims (1-4, 6 and 8-20) is not patentably distinct or non-obvious over the prior art of record in view of the reference(s), Isom. Therefore the rejection is maintained.

5. Copy of the office action rejection mailed on 8/14/2008 follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 6 and 8-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Isom, III et al. US patent no. 7055069 (Hereinafter Isom).

7. In regard to claim 1, Isom teaches:

method for testing an integrated circuit (IC) comprising:

employing one of a plurality of input lines coupled to a processor to receive a test signal for the processor wherein the processor is positioned internally with the IC;

(Note: Figure 3, reference characters (3020, (304), (204) and (206) in Isom)

employing one of a plurality of output lines coupled to a processor to send a test result from the processor wherein the processor is positioned internally with the IC; and

(Note: Figure 3, reference characters (3020, (304), (204) and (206) in Isom)

if the test result is unsuccessful, performing at least one of:

selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

8. In regard to claim 2, Isom teaches:

The method of claim 1 wherein employing one of the plurality of input lines to

receive the test signal for the processor includes:

applying the test signal to each of the plurality of input lines;

selecting one of the plurality of input lines; and

receiving the test signal for the processor from the selected input line.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

9. In regard to claim 3, Isom teaches:

The method of claim 1 wherein employing one of the plurality of output lines to send the test result from the processor includes:

applying the test result to each of the plurality of output lines;

selecting one of the plurality of output lines; and

sending the test result from the processor using the selected output line.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

10. In regard to claim 4, Isom teaches:

The method of claim 1 wherein employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

• selecting a remaining one of the plurality of input lines; and • employing the selected remaining one of the plurality of input lines to receive the test signal.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

11. In regard to claim 6, Isom teaches:

The method of claim 1 wherein employing a remaining one of the plurality of output lines to send the test result from the processor includes:

selecting a remaining one of the plurality of output lines; and

employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

12. In regard to claim 8, Isom teaches:

(Original) The method of claim 1 wherein:

employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

selecting a remaining one of the plurality of input lines; and

employing the selected remaining one of the plurality of input lines to receive the test signal; and

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

employing a remaining one of the plurality of output lines to send the test result from the processor includes:

selecting a remaining one of the plurality of output lines; and

employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

13. In regard to claim 9, Isom teaches:

The method of claim 8 wherein:

selecting a remaining one of the plurality of input lines includes:

modifying a first select signal; and

selecting a remaining one of the plurality of input lines based on the modified first select signal; and

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

selecting a remaining one of the plurality of output lines includes:

modifying a second select signal; and

selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

14. In regard to claim 10, Isom teaches:

An apparatus for testing an IC comprising:

a processor within the IC;

(Note: Figure 3, ref (206) in Isom)

a plurality of input lines coupled to the processor positioned internally within the IC;

(Note: Figure 3, ref (102) in Isom)

a plurality of output lines coupled to the processor positioned internal within the IC; and

(Note: Figure 3, ref (102) in Isom)

a connector interface coupled to the plurality of input lines and the plurality of output lines; wherein the apparatus is adapted to:

(Note: Figure 3, ref (202) in Isom)

employ one of the pluralities of input lines to receive a test signal for the processor;

(Note: Figure 3, ref (102) in Isom)

employ one of the plurality of output lines to send a test result from the processor; and

(Note: Figure 3, ref (102) in Isom)

if the test result is unsuccessful, perform at least one of:

selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

(Note: Figures 4 & 5 and col. 7, lines (40-67) through col. 8, lines (1-6) in Isom)

15. In regard to claim 11, Isom teaches:

The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and

further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:

select one of the plurality of input lines; and

receive the test signal for the processor on the selected input line.

(Note: Figure 3, ref (310) in Isom)

16. Claim 13 ~s rejected for the same reasons as per claim 4.

17. Claim 14 ~s rejected for the same reasons as per claim 2.

18. Claim 15 ~s rejected for the same reasons as per claim 6.

19. Claim 16 ~s rejected for the same reasons as per claim 13.

20. Claim 17 ~s rejected for the same reasons as per claim 8.

21. Claim 18 ~s rejected for the same reasons as per claim 9.

22. Claim 19 ~s rejected for the same reasons as per claim 8.

23. Claim 20 ~s rejected for the same reasons as per claim 9.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free).

/Sam Rizk/

Examiner, Art Unit 2112

/Esaw T Abraham/

Primary Examiner, Art Unit 2112